STM8S Standard Peripherals

May 2009

STM8S Technical Training

Purpose

The purpose of this part is :

- To present you all the standard peripheral set, containing:
  - GPIO
  - ADC
  - Timers
- To focus on the new functionalities comparing to ST7

Objective

- At the end of this chapter you will be able to
  - Use GPIO, ADC and Timer
  - List all the features of standard peripherals
  - Configure peripherals according to your needs

STM8S General Purpose I/Os

GPIO Features (1/2)

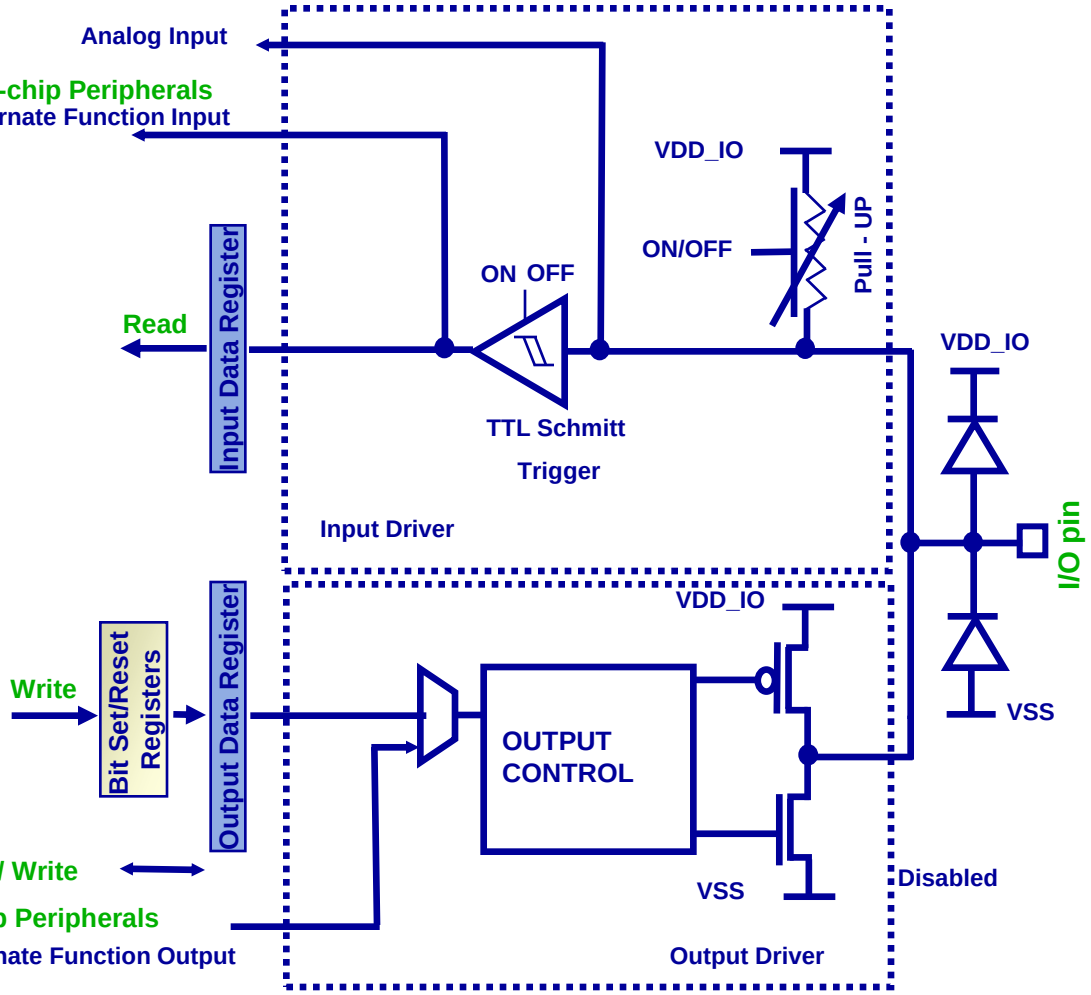
- 70 multifunction bi-directional I/O ports for the 80 pin package
  - Up to 70 Standard I/Os (3mA drive and 8mA for High-sink capable I/Os)
  - Up to 16 analog inputs
  - Up to 38 I/Os can be set-up as external interrupts including TLI (with sensitivity selection)
    - Up to 37 with wake-up capability
- All Standard I/Os are shared in 9 ports (GPIOA..GPIOI)
- Individually configurable (Direction, configuration, ext. int., slope …)
- Separate registers for data input and output
  - Allowing bit handling on the GPIO register

GPIO Features (2/2)

- Highly robust I/O design, immune against current injection
- some I/Os with 10 MHz toggling frequency capability
  - with output slope control for EMC noise reduction
- Alternate Functions pins (like USARTx, TIMx, I2Cx, SPIx, CAN, …)

GPIO Configuration Modes

Configuration Mode	DDR	CR1	CR2 / ADCTDR
Analog Input	0	0	CR2 = 0 ADCTDR =1
Input floating	0	0	With interrupt capability if set
Input Pull-up	0	1	
Open-drain output	1	0	Speed limited to 10MHz if set
Push-pull Output	1	1	
True Open-drain	1	X	X



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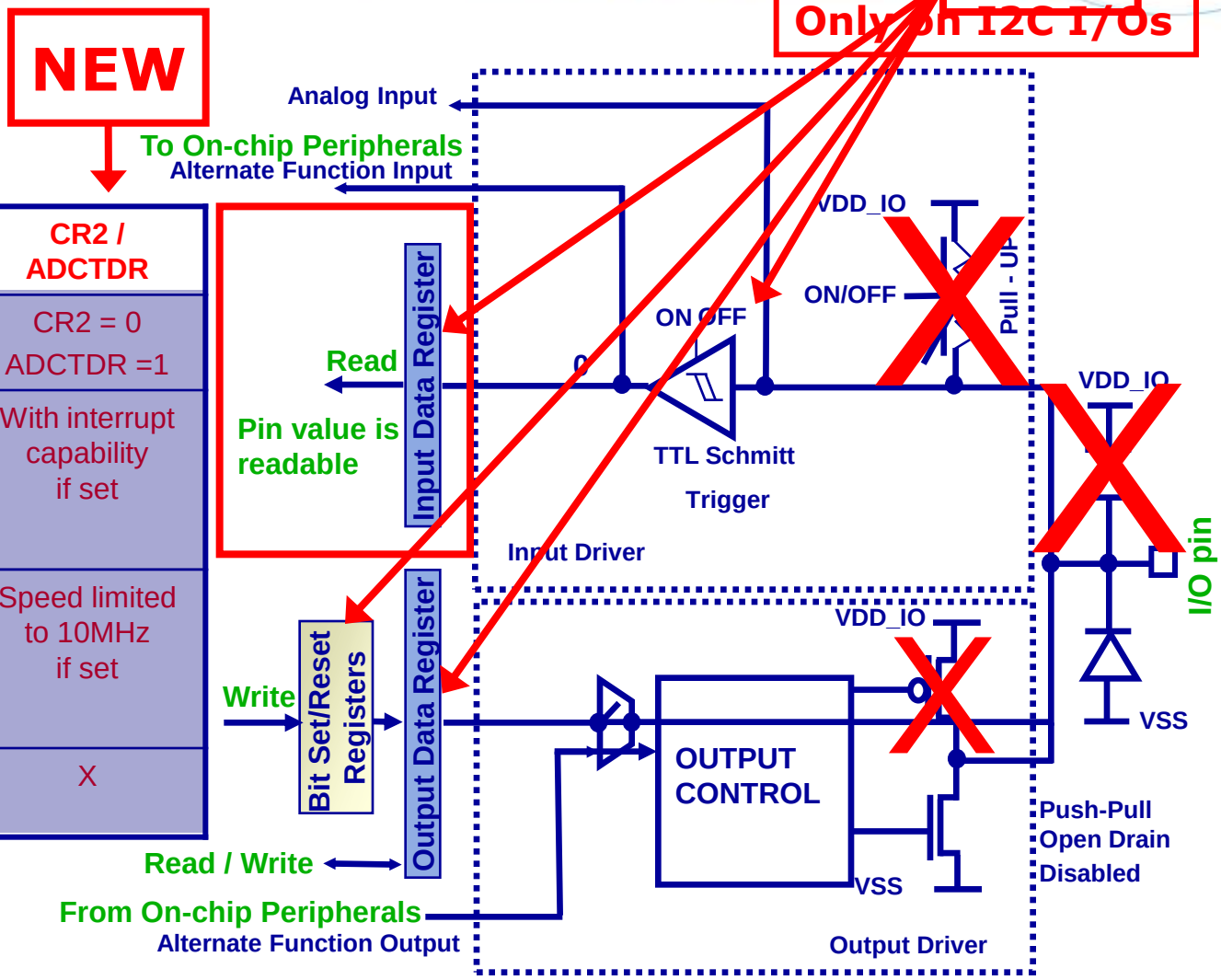


Programming Tips for GPIOs (1)

- A/D conversion
  - Each pin used by the ADC cell must be configured as floating input (i.e. without pull-up resistors) before activating the analog input mode (which is the usual default state)
- Alternate function
  - A signal coming from an on-chip peripheral can be output on a port. In this case, the I/O is automatically configured in output mode through Px_DDR
  - A signal coming from an I/O can be an input to an on-chip peripheral. In this case, it must be configured according to the peripheral.

WARNING

Peripherals do not modify the complete I/O configuration: Px_CR1 registers are not forced by hardware

YOU NEED TO MANAGE Px_CR1 BY SOFTWARE

Programming Tips for GPIOs (2)

- Open Drain Outputs can be used for bus driving where several devices are connected on the same line (to avoid conflicts: lines can be pulled low or in high impedance) .
- I/Os can be wired together in parallel to increase current drive capability
- Voltages driving an Analog Input should always stay within the absolute maximum ratings (Vss-0.3V to Vdd+0.3V)
- Pull-up resistors typically 45kOhm

Quiz

- What is the equivalent name of the ST7 option register (OR)?
- How to enable the external interrupt on STM8 ?

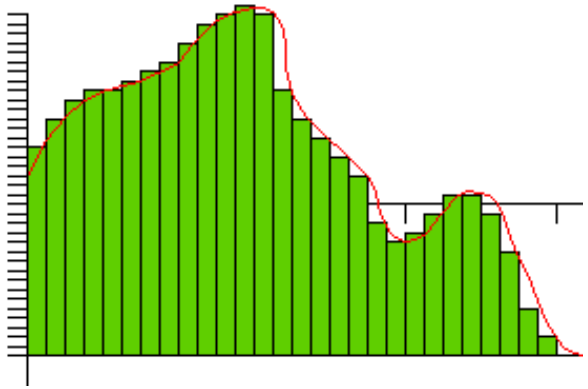
R

- What is the use of limiting the transition slope when GPIO is configured in output ?
- Which instruction can be now used on Px_ODR and should not be used on ST7 DR register ?

STM8S ADC

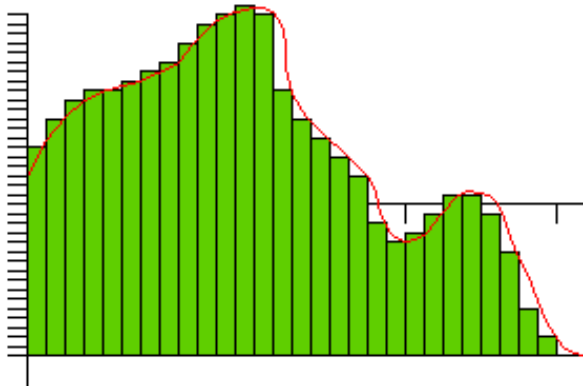
ADC Features

- Two type of ADCs, ADC1 and ADC2 - check your datasheet
- Common features
  - 10 bit resolution
  - 16 multiplexed input channels
  - Conversion time 3.5 µs min
  - ADC clock range: 1 to 4 MHz
  - Input range Vref- < Vin < Vref+
  - Vref- range 0 to 0.5V; Vref+ range 2.75 to Vdda
  - External trigger and timer trigger selection
  - Single or continuous conversion modes
  - End of conversion interrupt
  - Data alignment – left and right
  - Clock prescaling

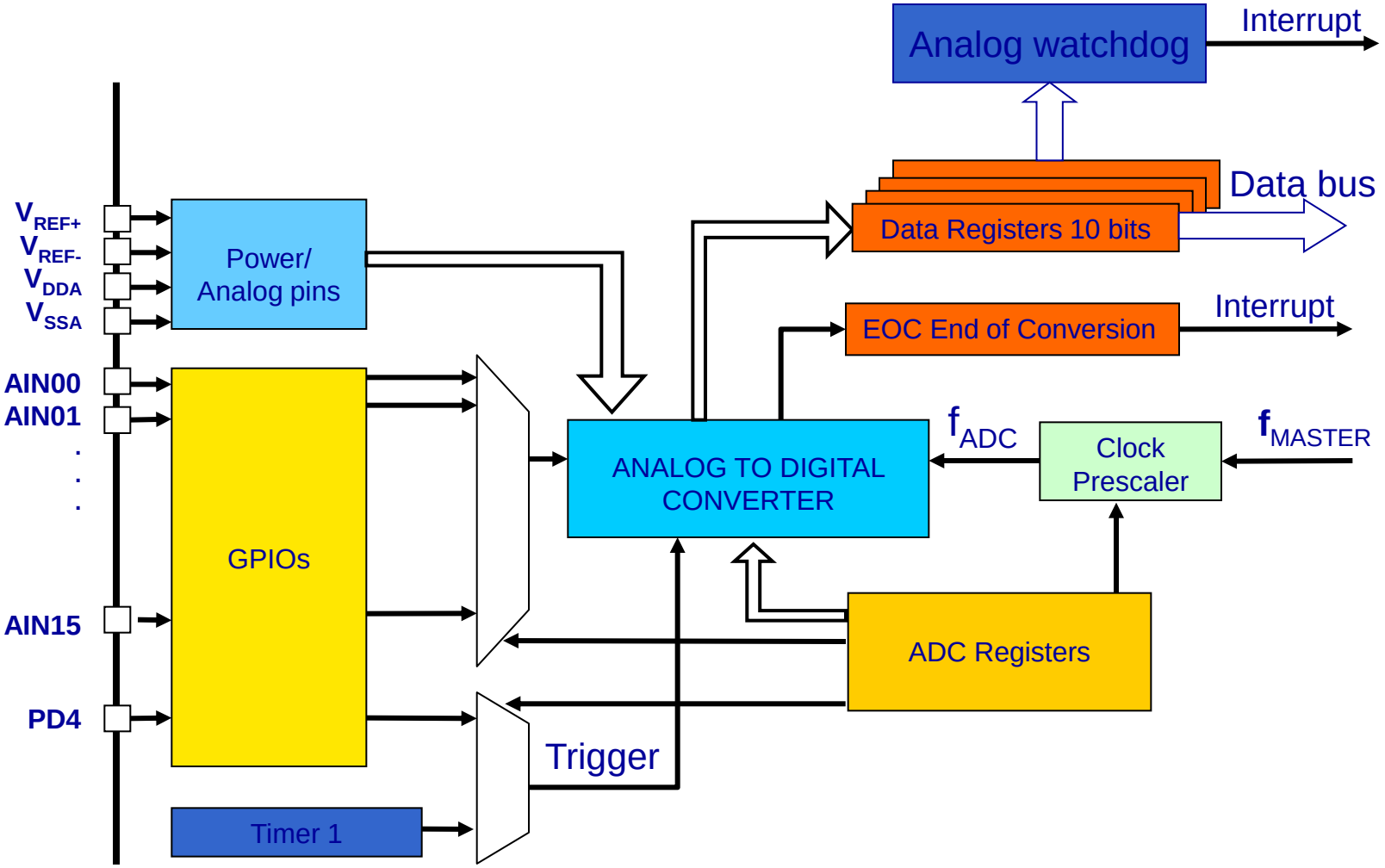


ADC1 Features

- Some features are available only on ADC1
  - Scan mode
    - single scan
    - continuous scan
  - Buffered continuous mode
    - Overrun flag
  - Analog watchdog 10 channels, 10 bits
    - low and high thresholds
  - Analog watchdog interrupt

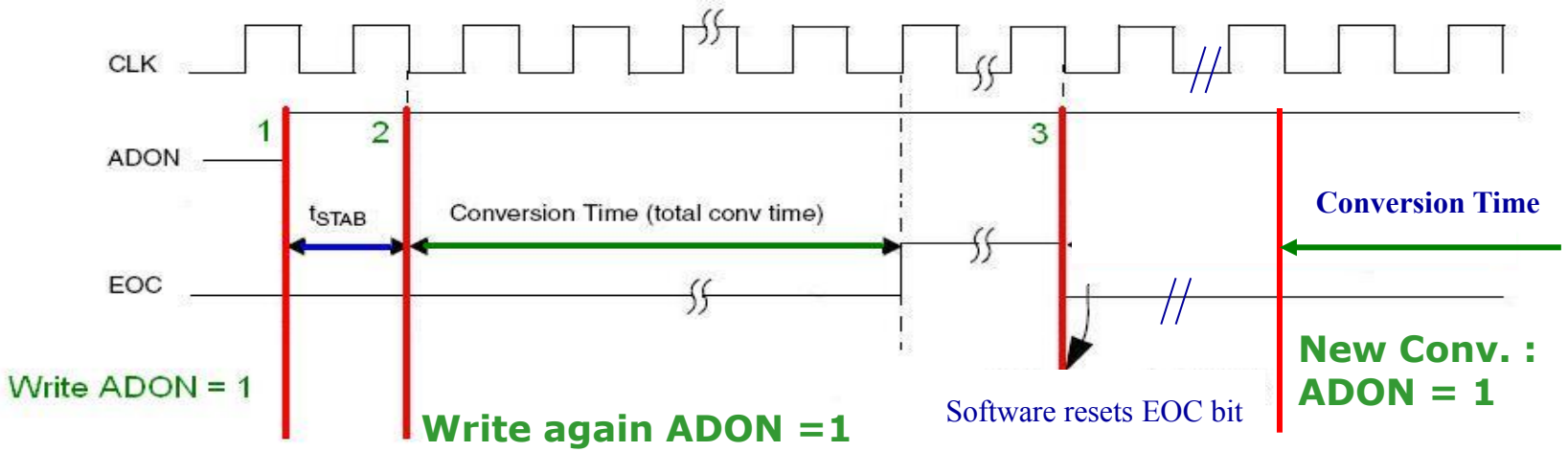


Block Diagram

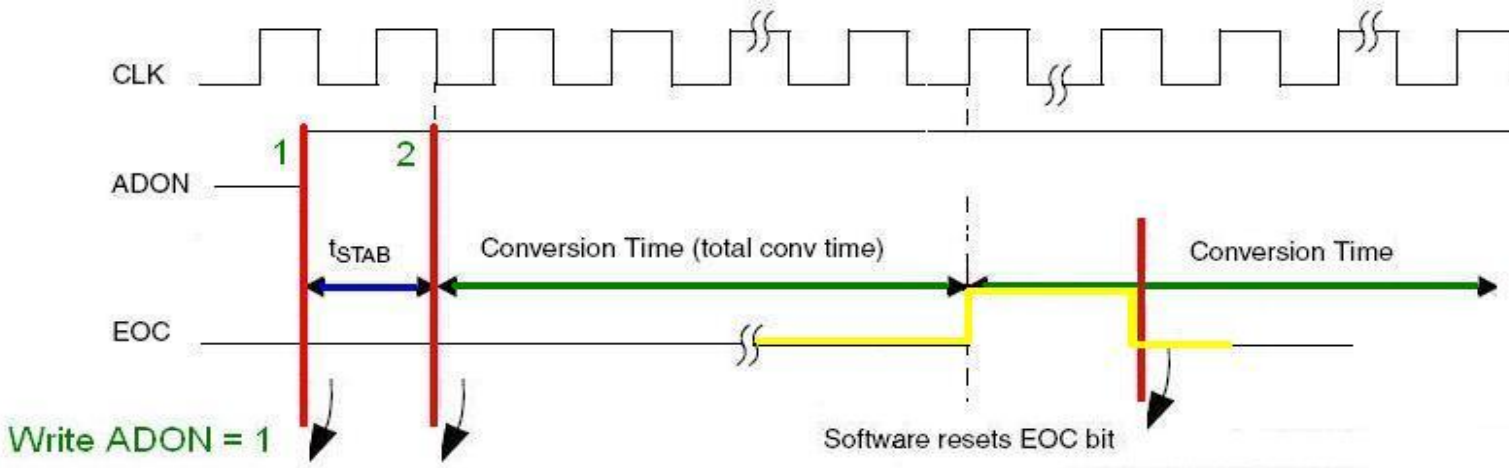


Conversion Modes

- **Single**

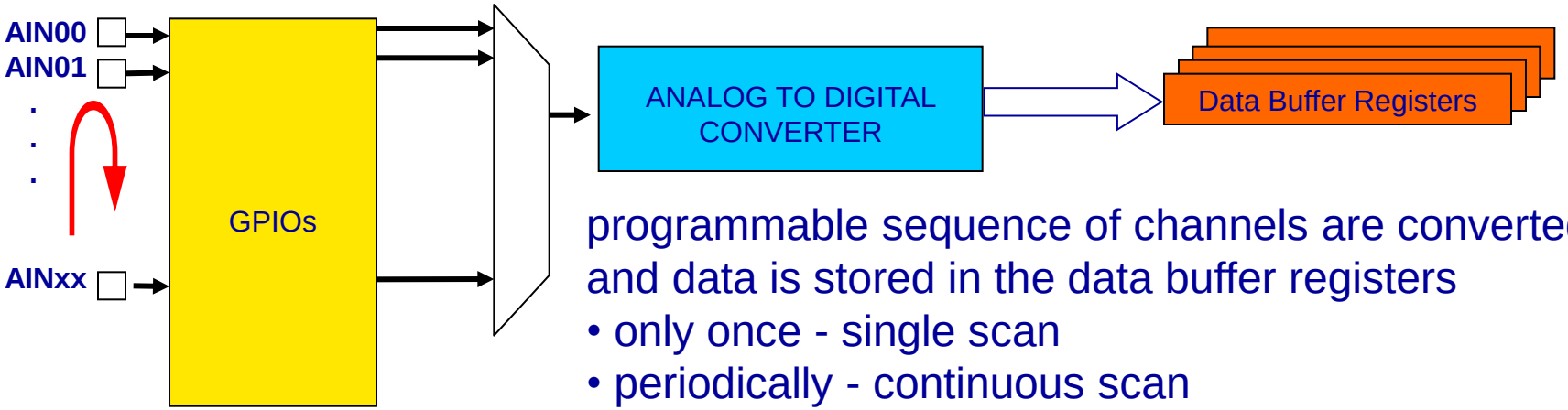


- **Continuous**



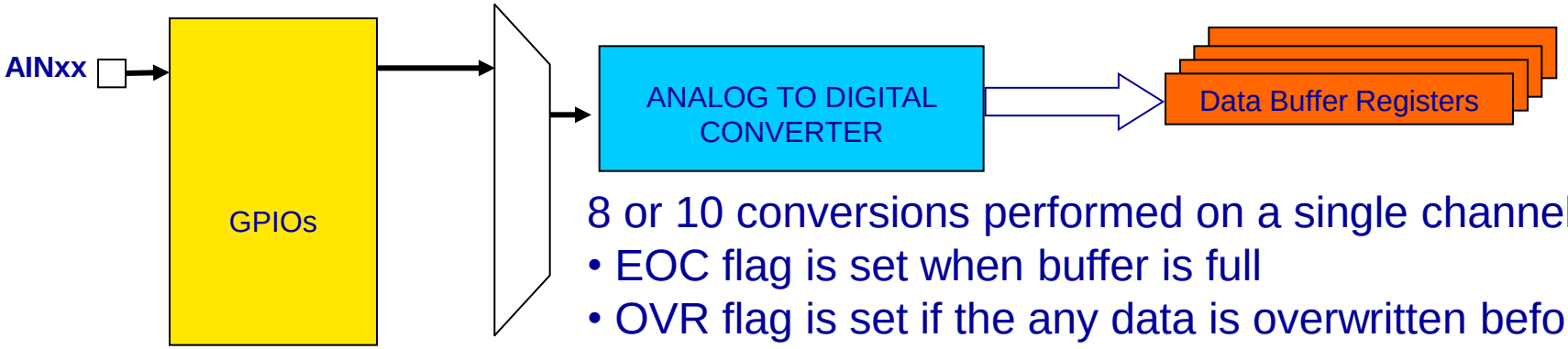
Conversion Modes - continue

- **Scan mode**



programmable sequence of channels are converted and data is stored in the data buffer registers
- only once - single scan
- periodically - continuous scan

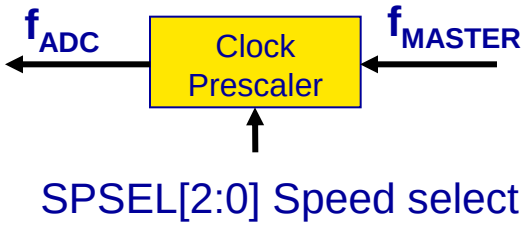
- **Buffered continuous mode**



8 or 10 conversions performed on a single channel
- EOC flag is set when buffer is full
- OVR flag is set if the any data is overwritten before it has been read

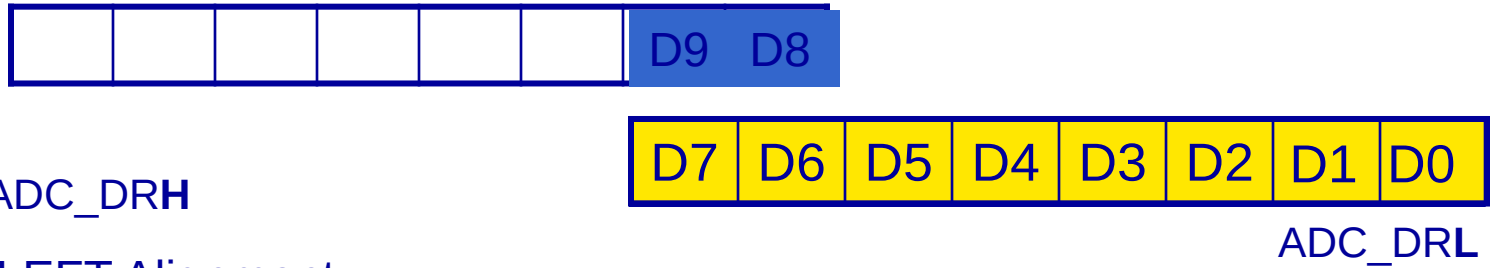
Clock Setting and Data Alignement

– **Clock prescaler**

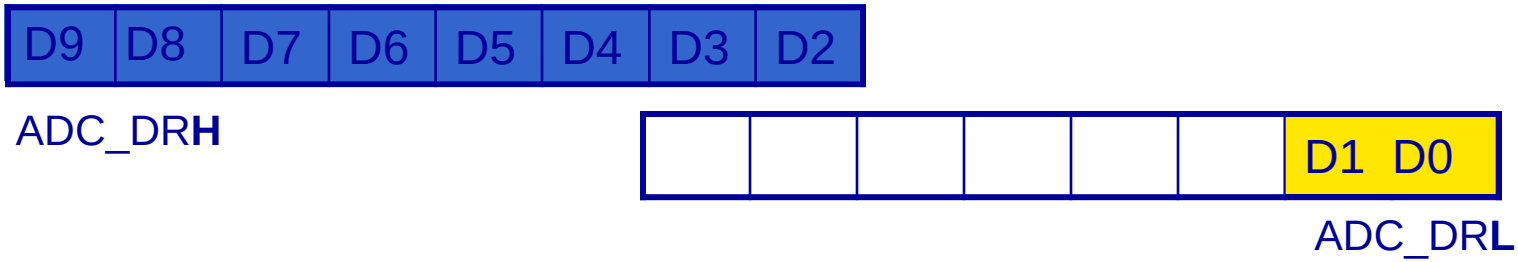


– **Data Alignment**

RIGHT Alignment

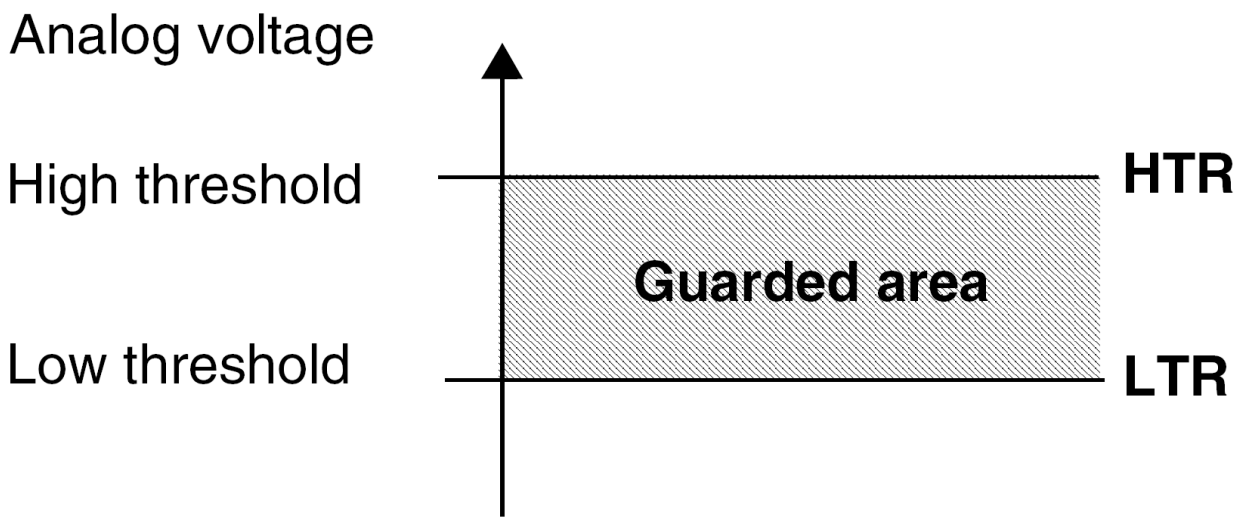


LEFT Alignment

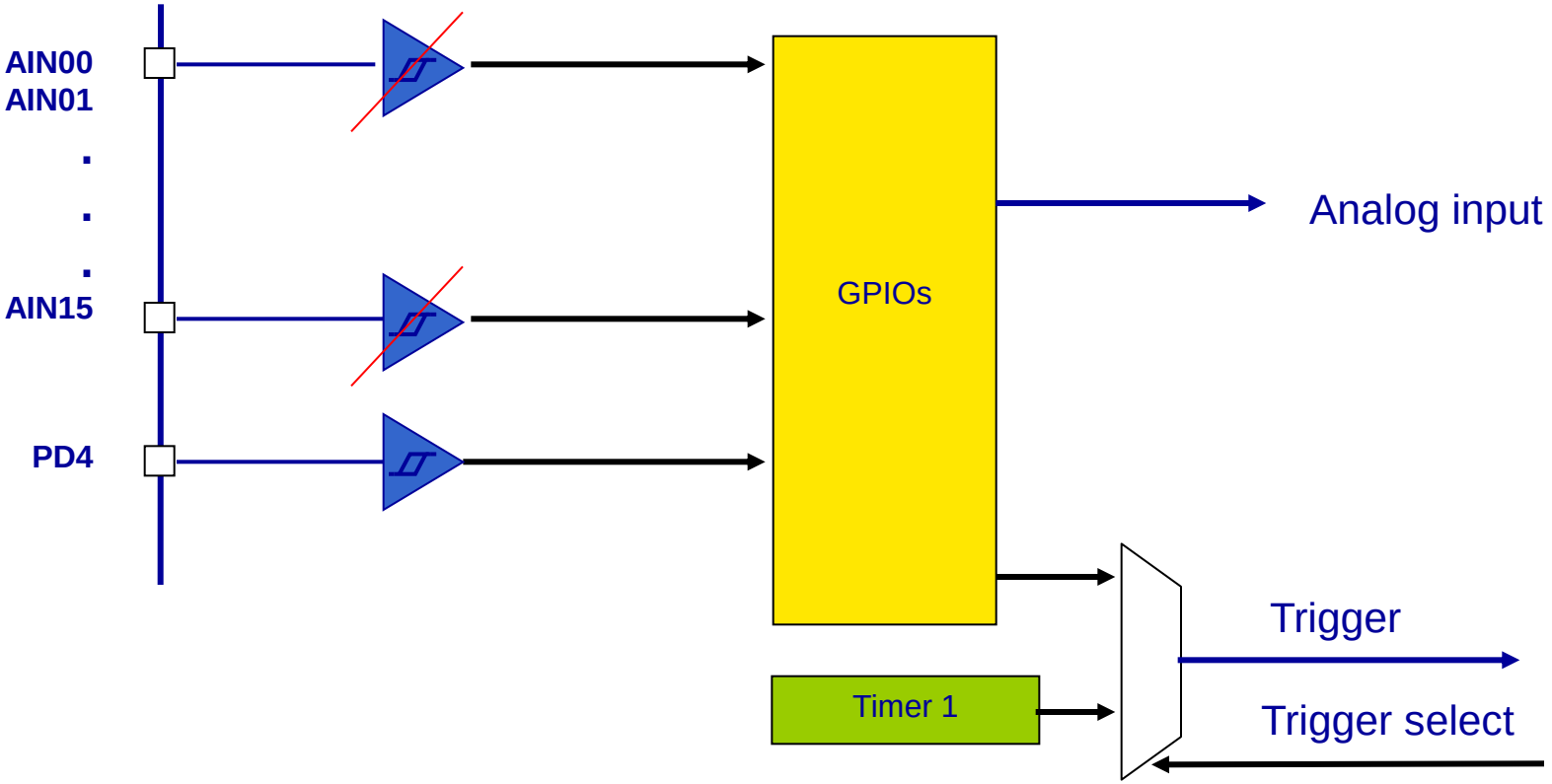


Analog watchdog

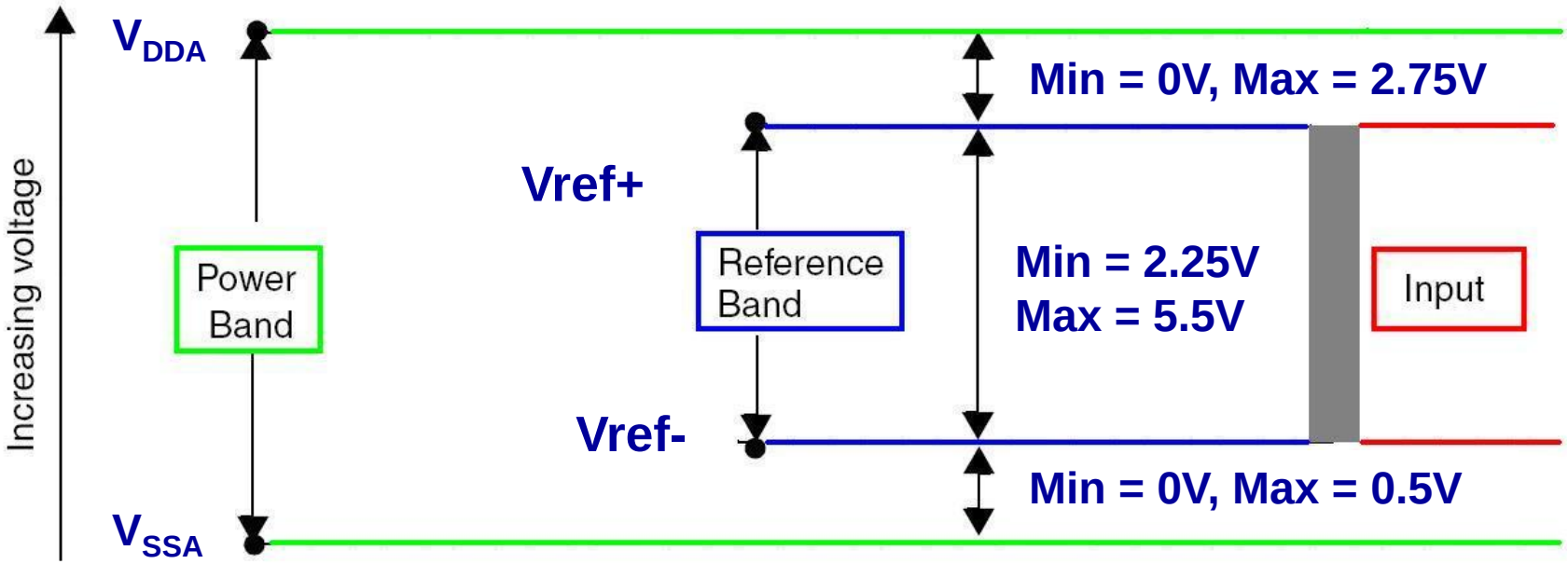
- 10 analog watchdog channels
- Independently programmable Low and High threshold for each channels
- Dedicated analog watchdog interrupt
- Enable for single conversion or non-buffered continuous conversion modes



Channel Selection
Conversion on External Trigger
Schmitt Trigger Selection



Analog zooming



Quiz

- What is the max clock frequency for ADC and what is the conversion time for maximum ADC clock?
- How can you trigger an analog conversion ?
- How should be configured the I/O which is used as ADC input channel?

STM8S TIMER PERIPHERALS

STM8S Timers

The STM8S device embeds 4 timer

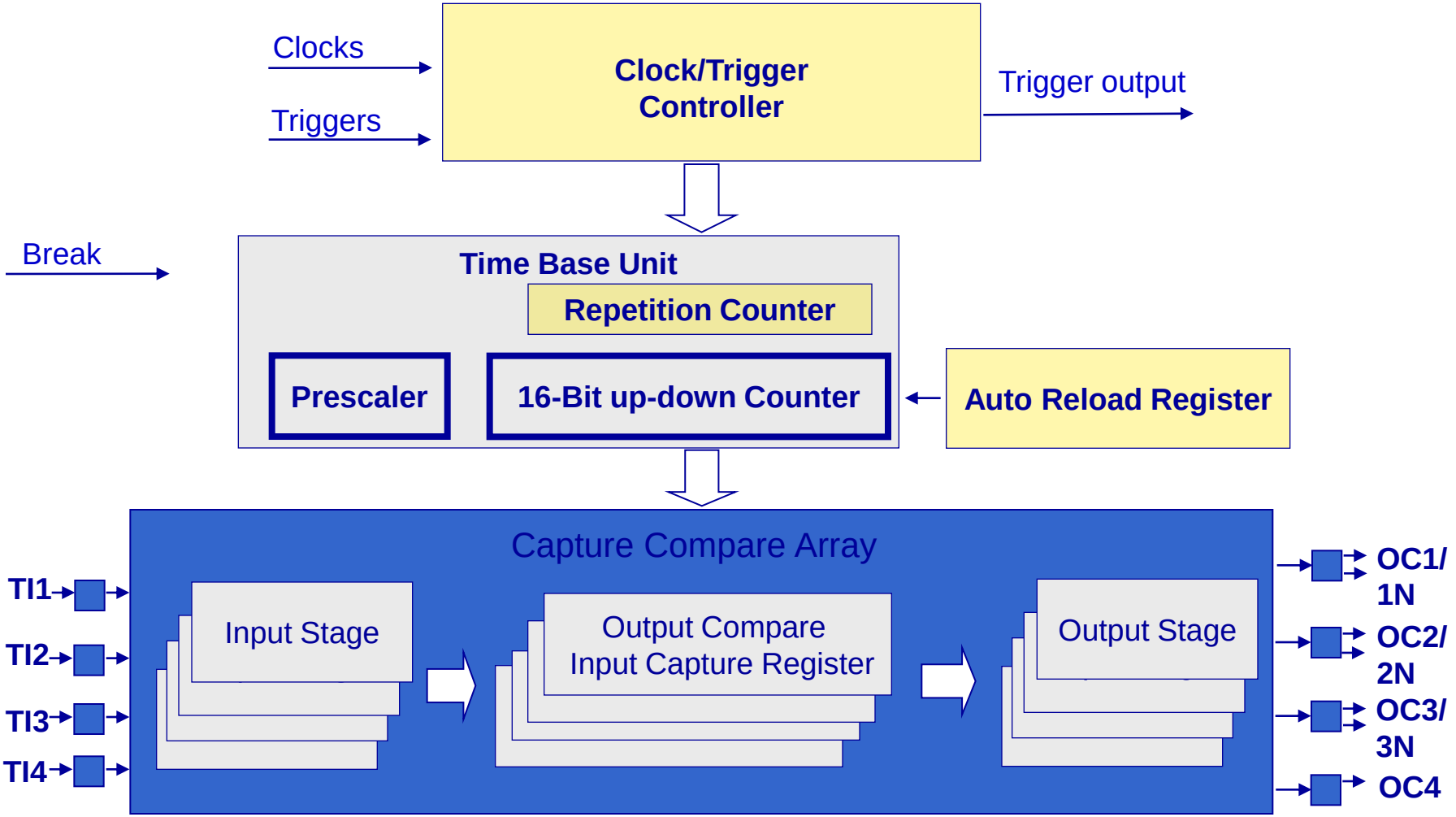
- Timer 1 – 16 bit, 4 channels, Motor Control timer
- Timer 2,3 – 16 bit, 3,2 channels, General Purpose timers
- Timer 4 – 8 bit, 0 channels, System timer

Timer	Counter resolution	Counter type	Prescaler factor	Channels	Comple-mentary outputs	Repet-ition counter	External trigger input	External break input
TIM1	16-bit	Up/down	Any integer from 1 to 65536	4	3	Yes	1	1
TIM2		Up	Any power of 2 from 1 to 32768	3	None	No	0	0
TIM3				2				
TIM4	8-bit		Any power of 2 from 1 to 128	0				

STM8S Timer 1 Features

- **16-bit Counter**
  - Up, down and centered (up&down) counting modes
  - Auto Reload
  - Programmable prescaler
  - Repetition counter
- **4 x 16 bit Channels**
  - Input Capture, PWM Input Capture
  - Output Compare, PWM outputs (edge or center-aligned)
  - One pulse mode output
  - Complementary outputs & Dead time, Forced output mode
  - *Encoder interface, Hall Sensors interface (MC)*
- **Synchronization**
  - Reset, Triggered or Gated modes
  - Break input
- **Interrupts & Update Event**
  - Counter overflow / underflow
  - Counter initialization
  - Trigger, Break, Commutation
  - Input capture, Output compare

General Block Diagram

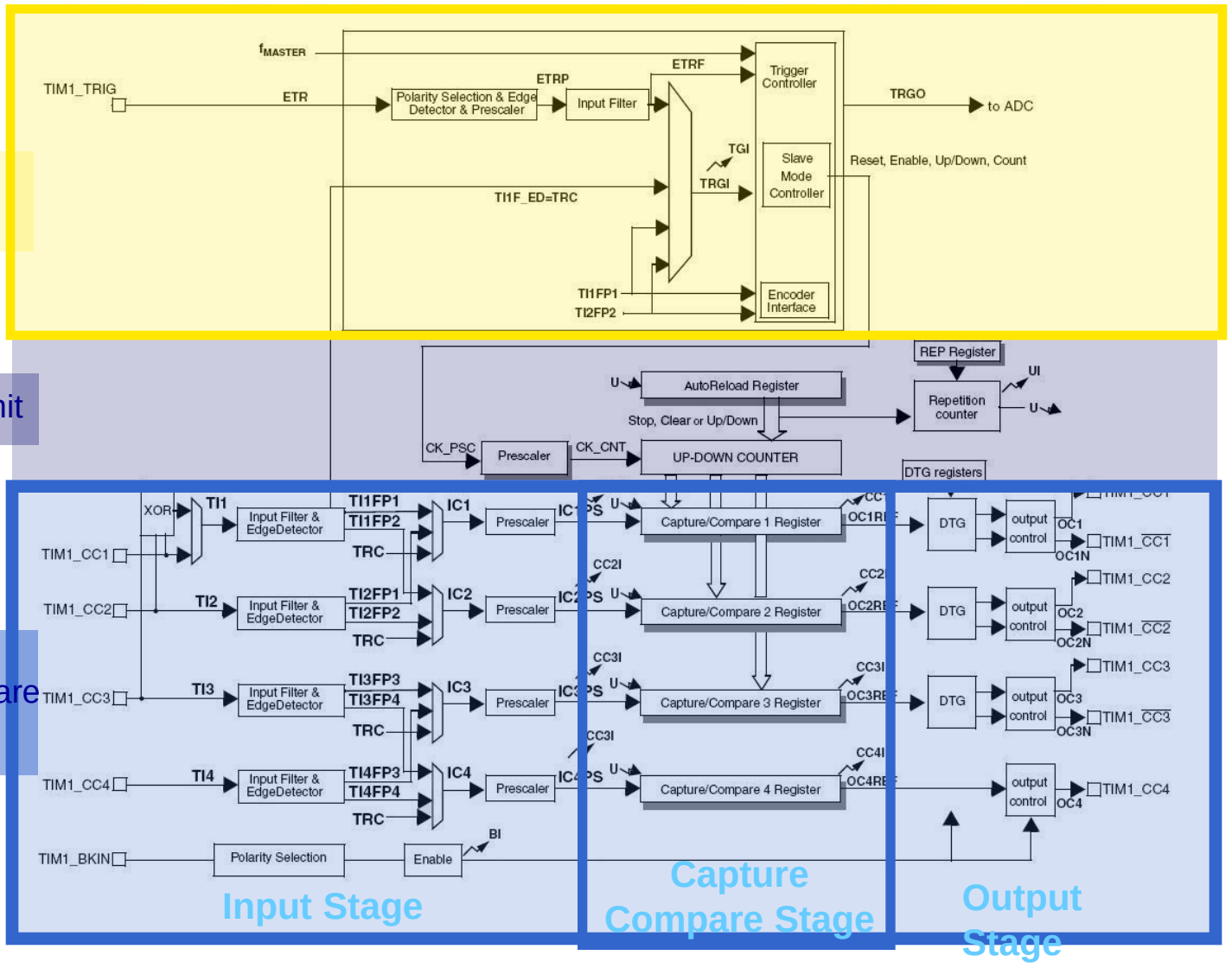


Block Diagram Details

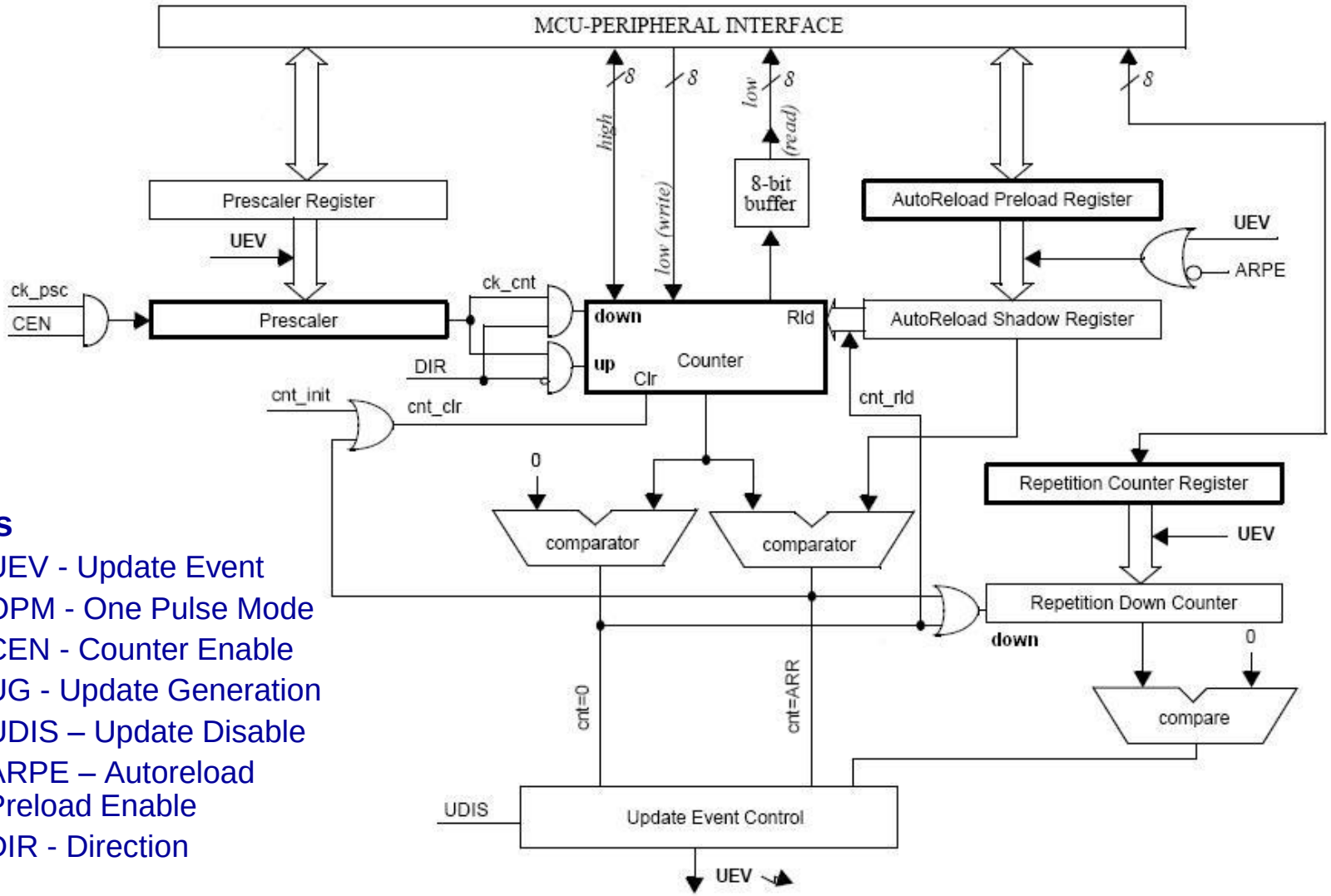
Clock/Trigger Controller

Time Base Unit

Capture/Compare Array



Time Base Unit: Block diagram



- **Notes**
  - UEV - Update Event
  - OPM - One Pulse Mode
  - CEN - Counter Enable
  - UG - Update Generation
  - UDIS – Update Disable
  - ARPE – Autoreload Preload Enable
  - DIR - Direction

Time Base Unit: Update Event (UEV)

The Update Event is used to trigger the transfer from the preload registers to shadow registers

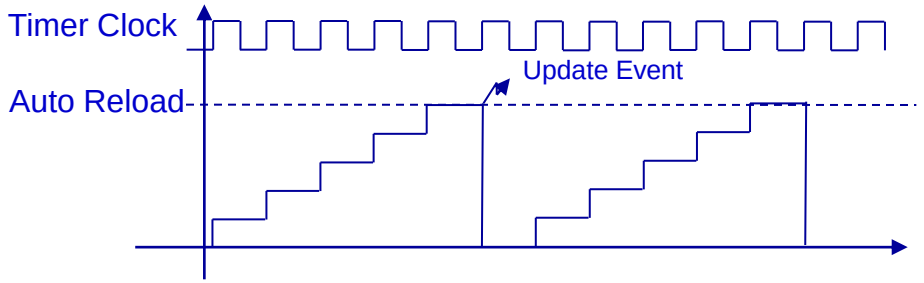
- **Registers with shadow:**
  - Prescaler
  - Auto Reload
  - Capture Compare (in Capture Compare Array)
  - Repetition Counter

- **Update Event is generated:**
  - on overflow or underflow event
  - when the counter is reinitialized
    - by software
    - by a trigger event

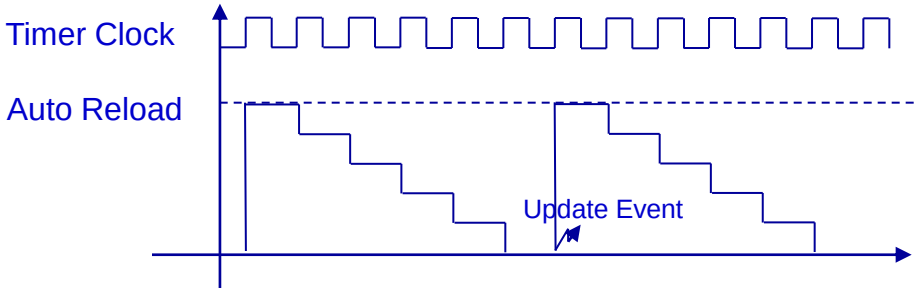
Time Base Unit: Counter Modes

EDGE-ALIGNED

- ✓ Up counting mode

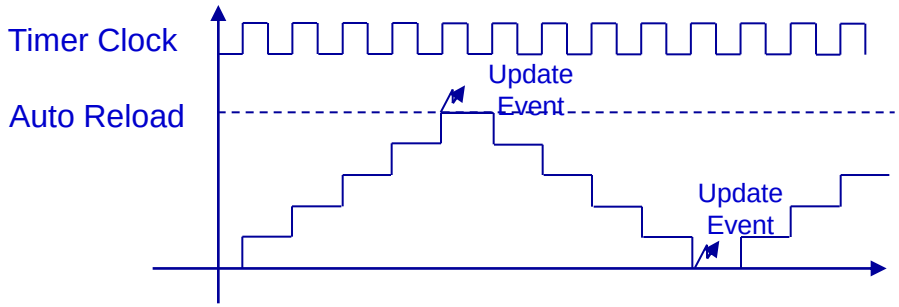


- ✓ Down counting mode



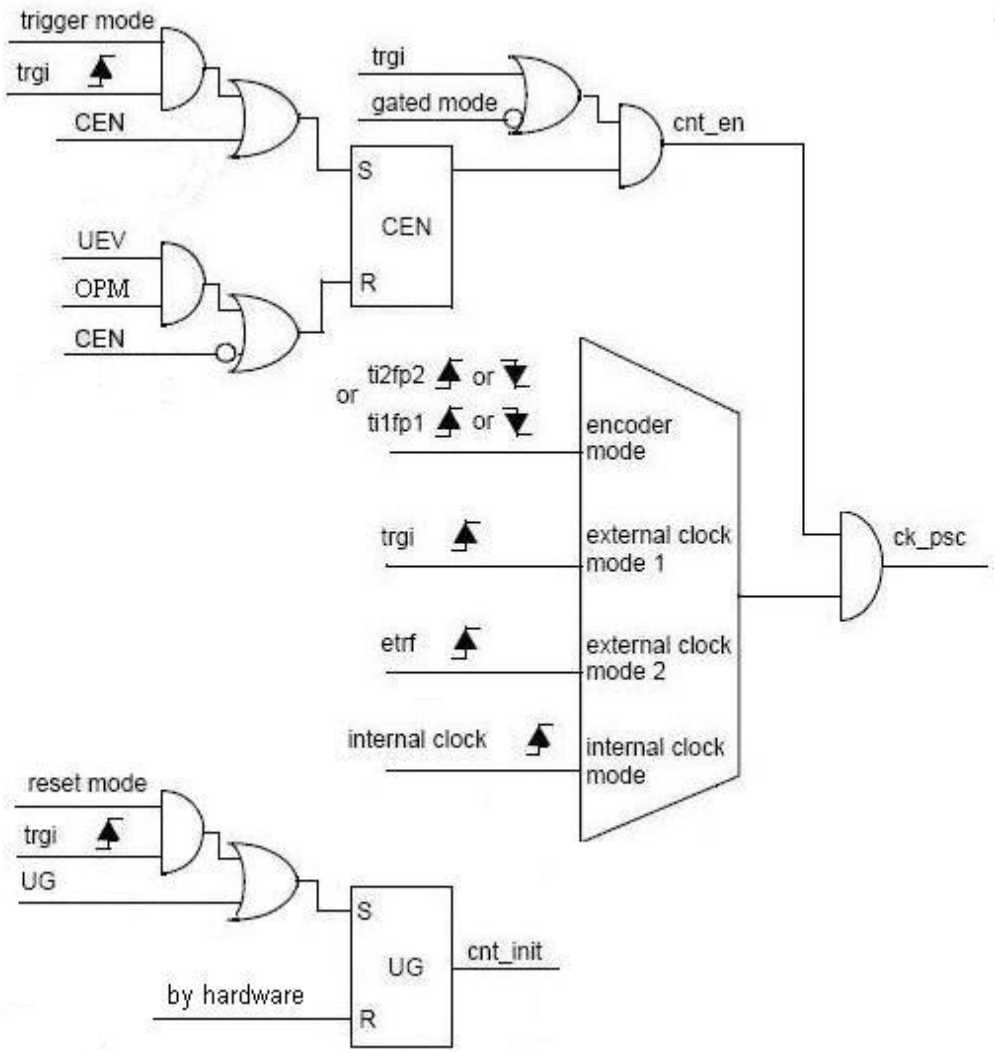
CENTER-ALIGNED

- ✓ Center-aligned mode



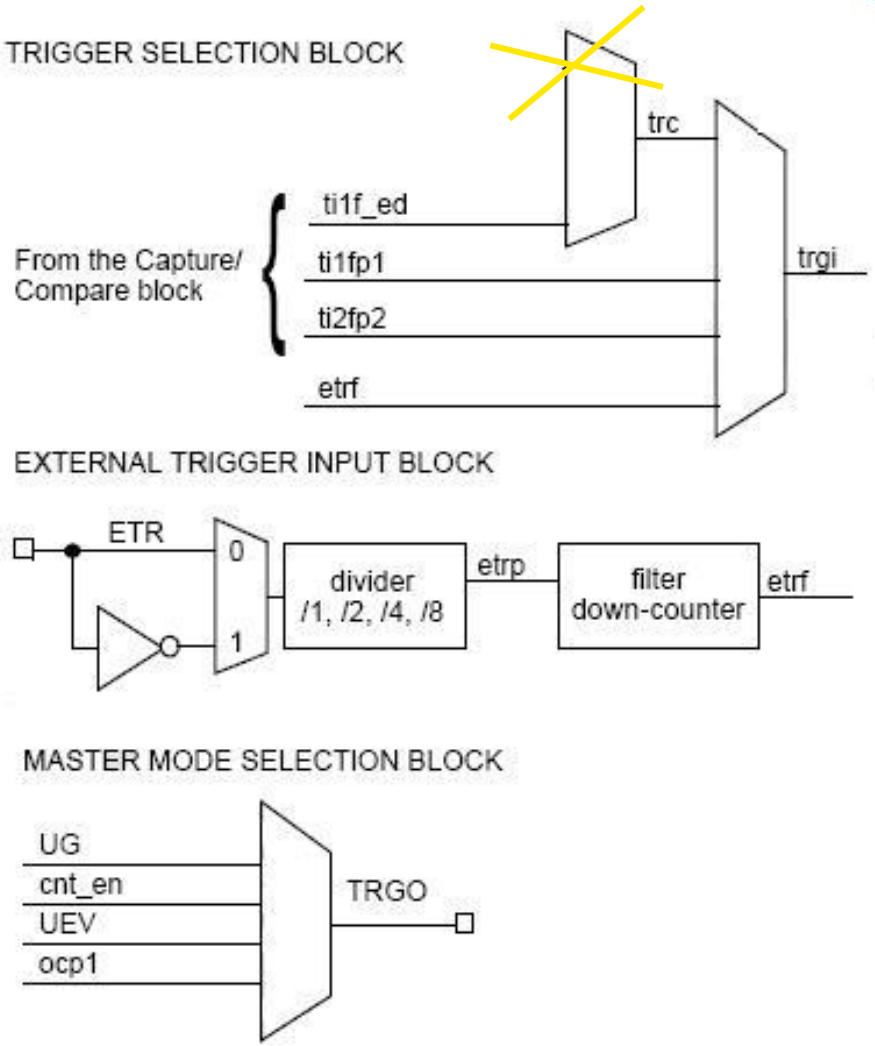
Clock Controller

- **Clock selection**
  - Internal clock (fMASTER)
  - External Timer Input pins, 1 &
  - External Timer Trigger input
- **Clock Trigger Modes:**
  - Trigger
  - Gated
  - Reset
- **Notes**
  - UEV - Update Event
  - OPM - One Pulse Mode
  - CEN - Counter Enable
  - UG - Update Generation



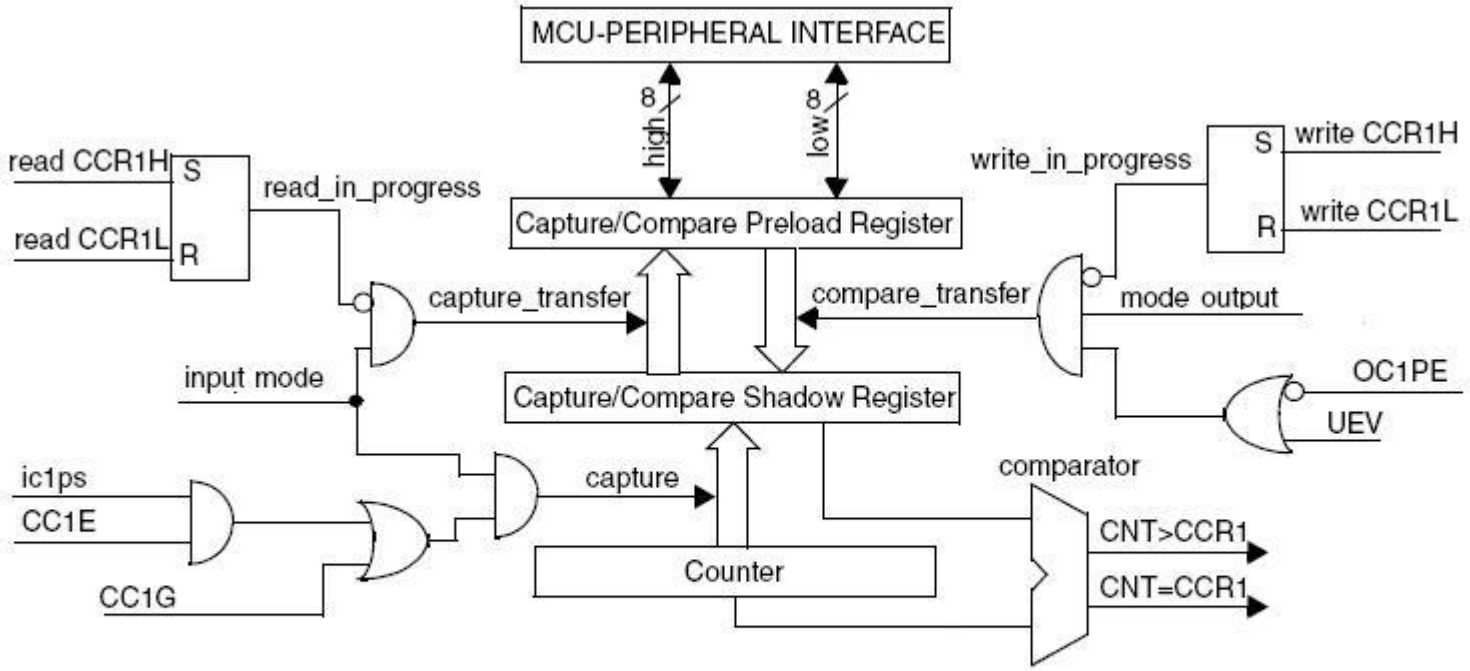
Trigger Controller

- **Trigger Input**
  - ETR
  - TI1
  - TI2



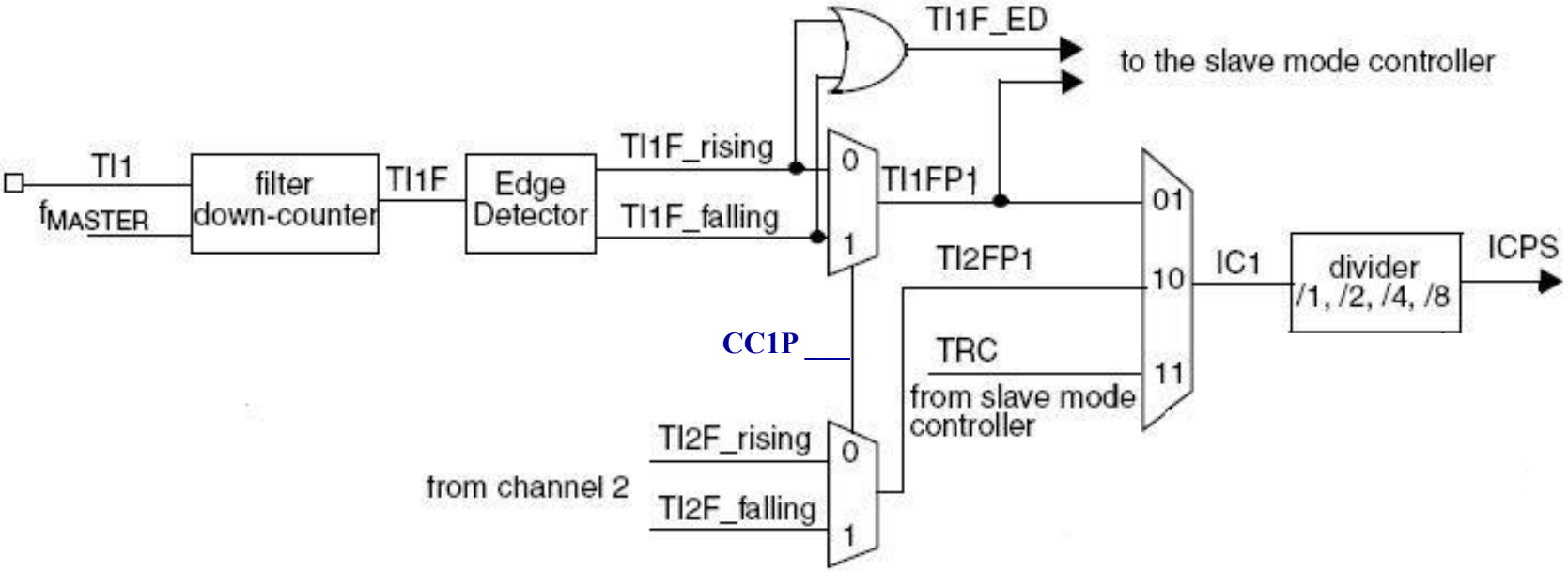
- **Trigger Output (ADC)**
  - Update Generation
  - Counter Enable
  - Update Event
  - Compare Pulse

Capture/Compare Array: Register Stage



- **Notes**
  - UEV - Update Event
  - CC1E – Capture Enable
  - CC1G – Capture Generation
  - OC1PE – Preload Enable
  - CCRx – Capture/Compare Register

Capture/Compare Array: Input Stage

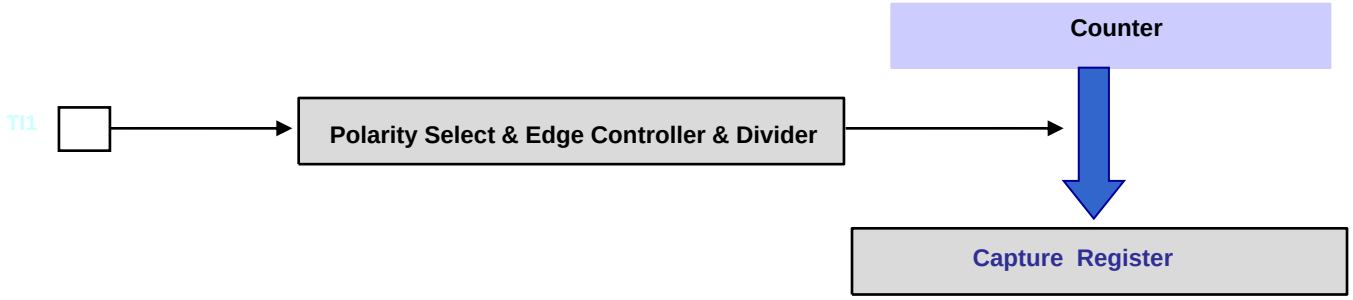


- Filtering
- Edge Detection
- Trigger selection
- Capture Selection
- Dividing

Input Capture Mode

Input capture registers are used to latch the value of the counter after a transition detected by the corresponding Input Capture pin.

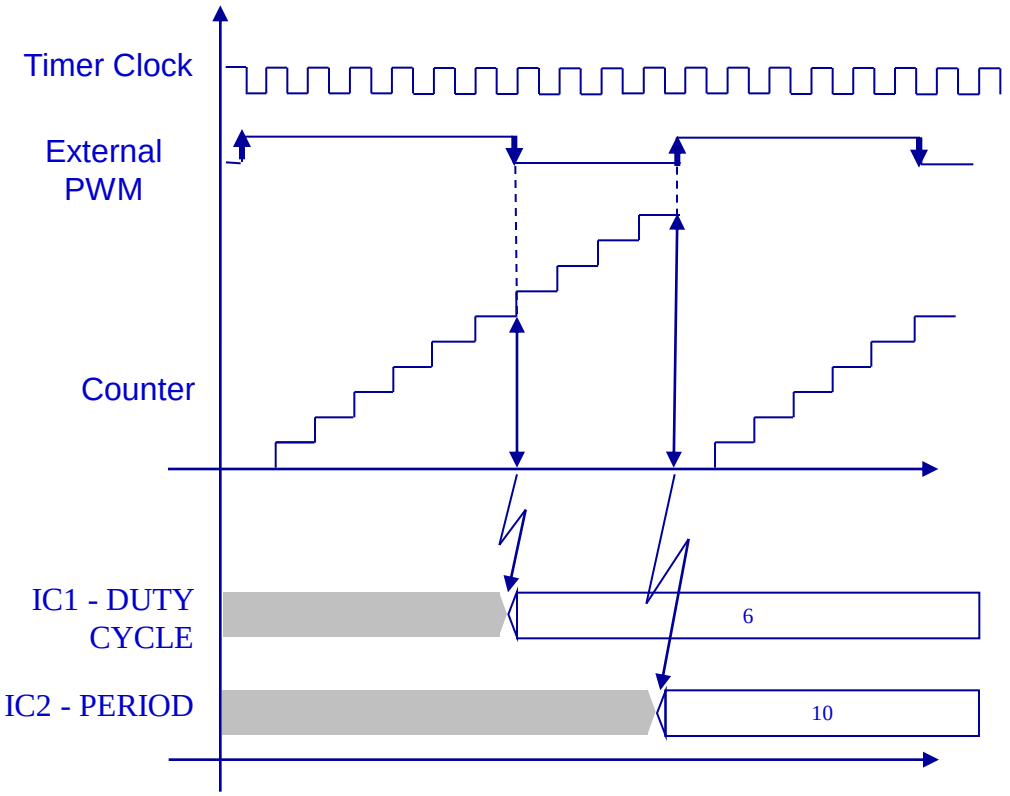
- Configure:
  - Source
  - Filter duration
  - Polarity selection
  - Edge Detection
  - Divider



PWM Input Mode

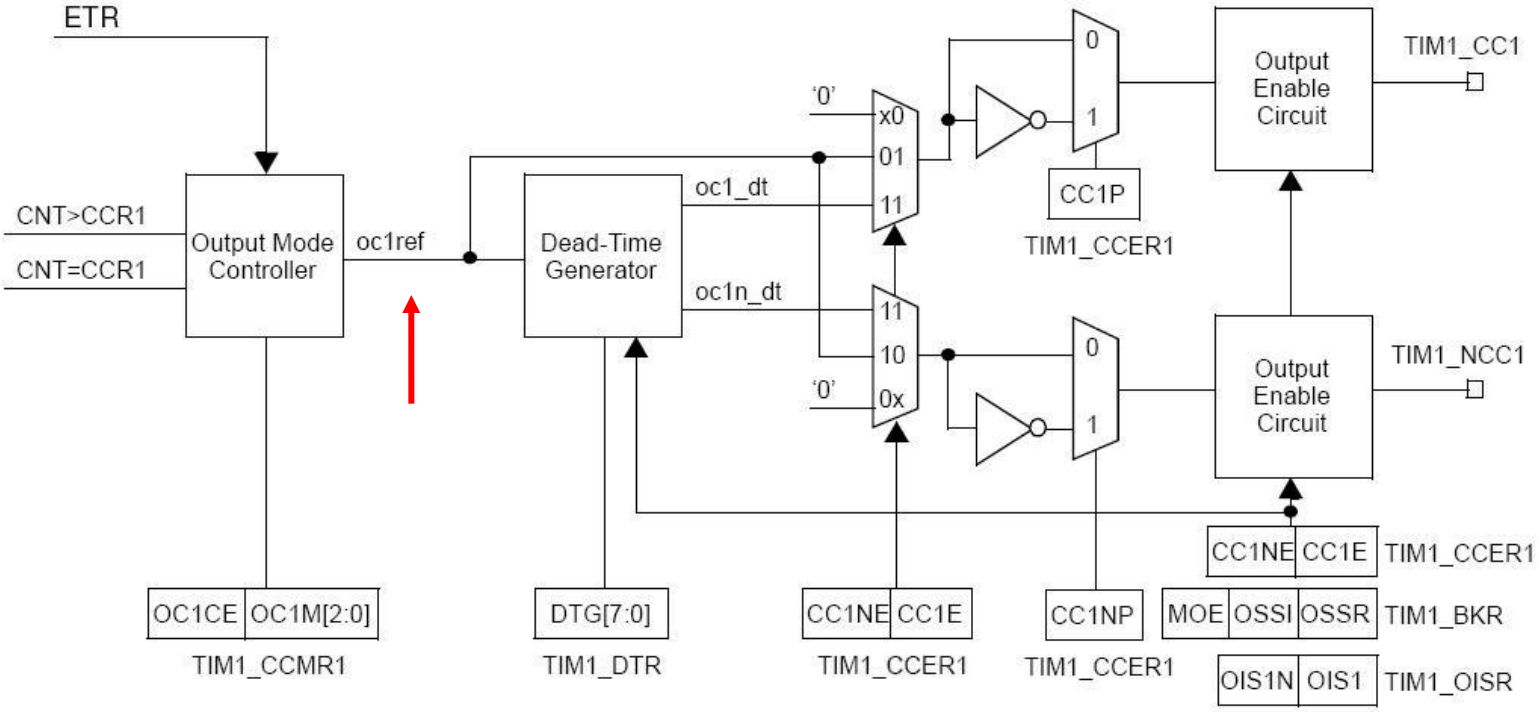
Enables the measurement of the **period** and the **pulse width**

- **Rising edge**: resets the counter and capture period
- **Falling edge**: capture duty cycle



Capture/Compare Array: Output Stage

- Output Compare Clear
- Output Compare Mode
- Dead Time
- Polarity
- Output State and Enable



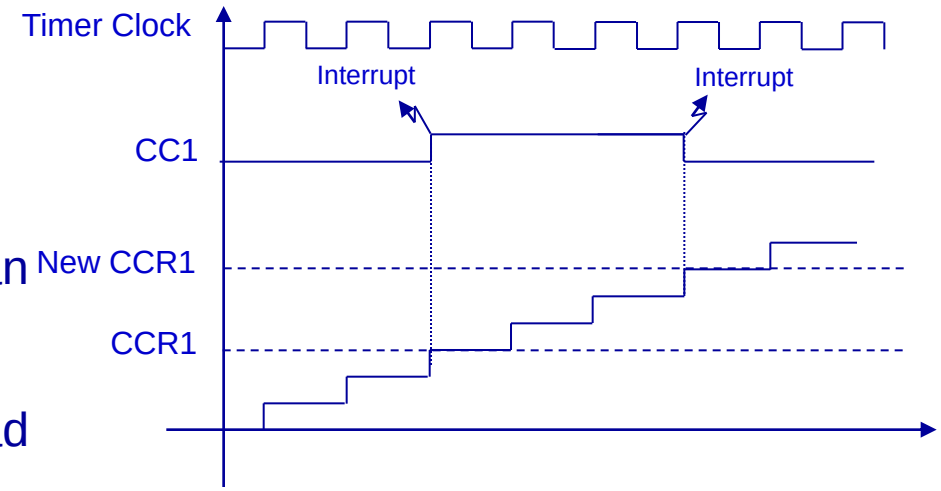
Output Compare Mode

Used to control an **output waveform** or indicate when a period of **time has elapsed**.

• When a **match** is found between the **Compare register** and the **counter**, the output pin can be programmed as:
  – Set
  – Reset
  – Toggle
  – Remain unchanged

• Generates an interrupt

• Output Compare register update can be configured as:
  – Immediate
  – On update event (Auto-reload update)

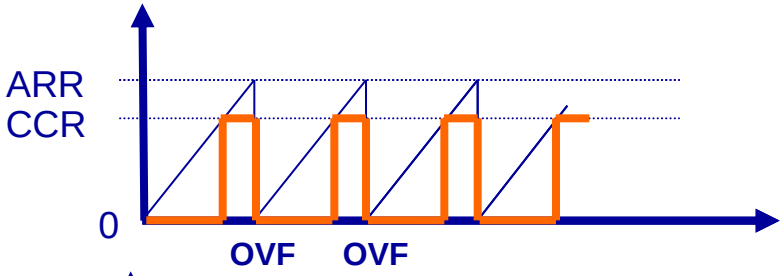


PWM Modes

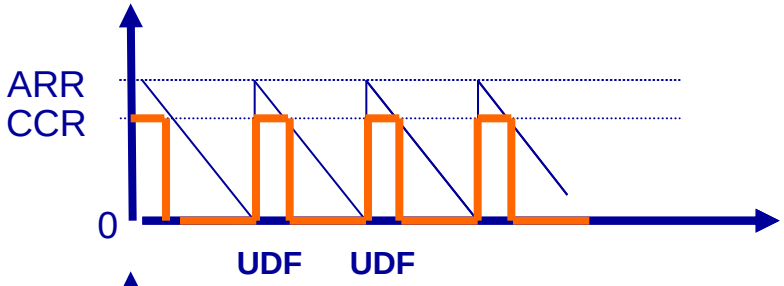
Generate independent signals with programmable frequency and a duty cycle

- Auto-reload register (ARR) define
  - the PWM period in Edge-Aligned mode
  - Half PWM period in Center-Aligned mode
- Each PWM channel has a capture compare register (CCR) to define the duty cycle

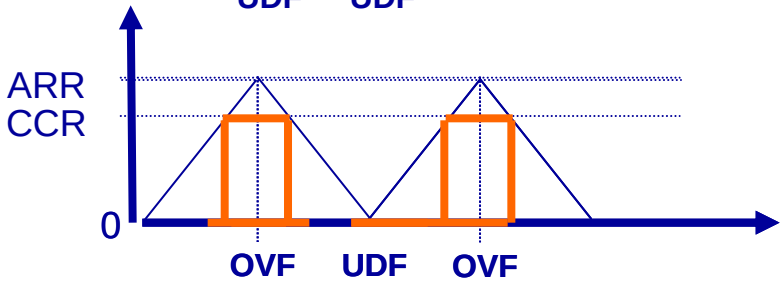
Edge-Aligned Up counting mode



Edge-Aligned Down counting mode



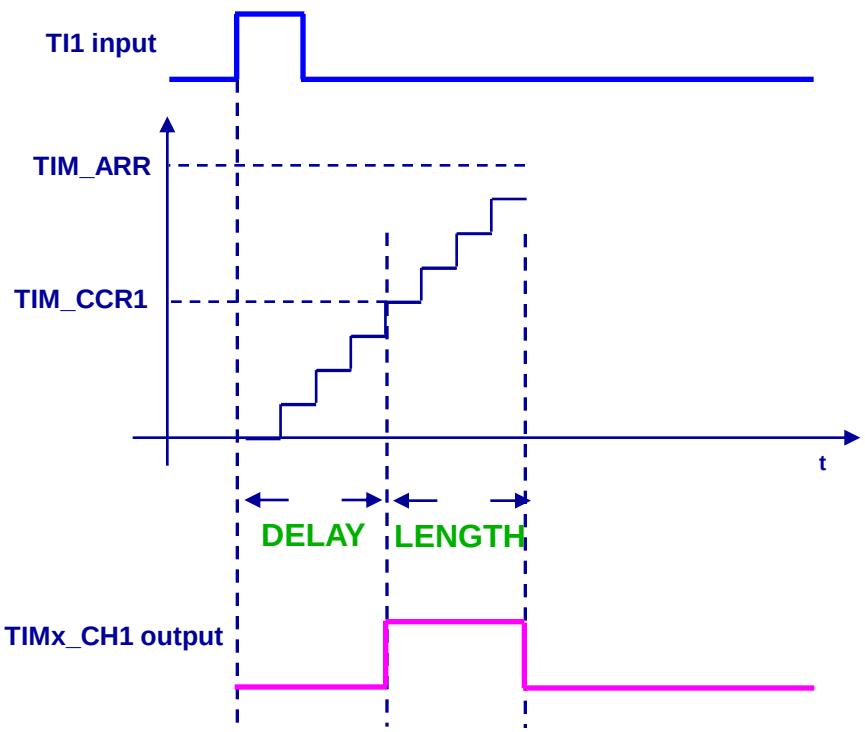
Center-aligned mode



One Pulse Mode

Generate a pulse with a programmable **length** after a programmable **delay** as **response to a stimulus**

- **Delay** defined by Output Compare register value
- **Length** defined by the difference between Auto Reload register value and Compare value



- There are two One Pulse Modes
  - Single Pulse
  - Repetitive Pulse - defined by repetition counter

Break Function

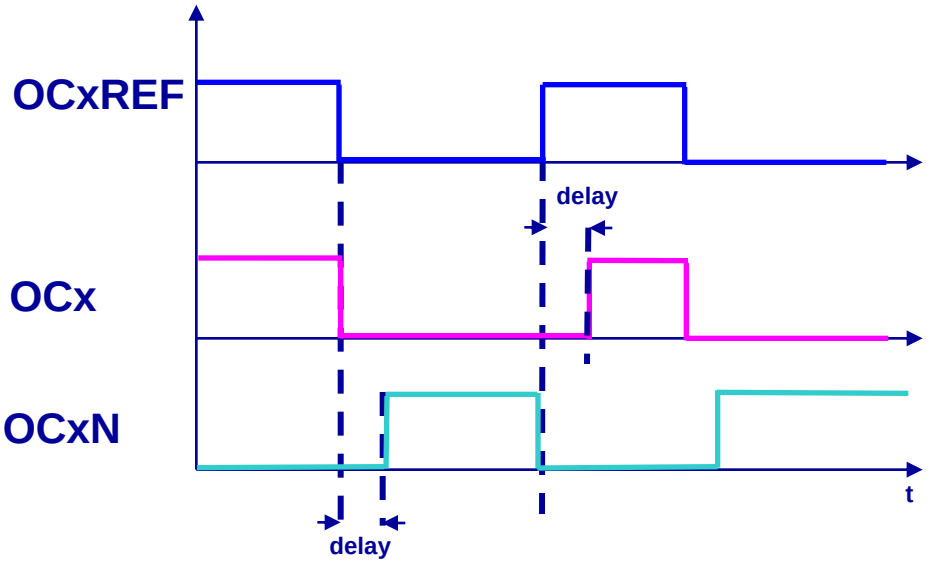
- **When a break occurs**
  - Main Output Enable is cleared - outputs are put to **programmable save state** even MCU oscillator is off
  - The break status flag is set and an interrupt can be generated
- **The break is generated by**
  - Hardware - input which has a programmable polarity
- **Automatic Output Enable**
  - If the Automatic Output Enable (AOE) is set, the MOE bit is automatically set again at the next update event UEV

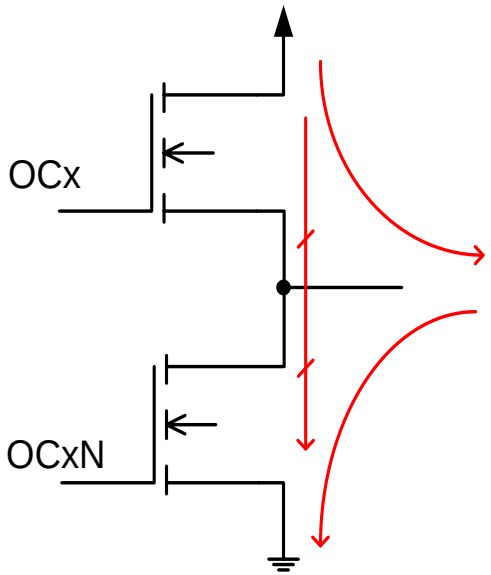
    This can be used to perform a **regulation**.
  - If the AOE is Reset, the MOE remains low until you write it to '1' again

    It can be used for **security**. The break input can be connected to an alarm from power drivers, thermal sensors or any security components.
- **Break Safeguard Circuit**
  - Write protection to freeze break configuration
  - 3 levels of protection

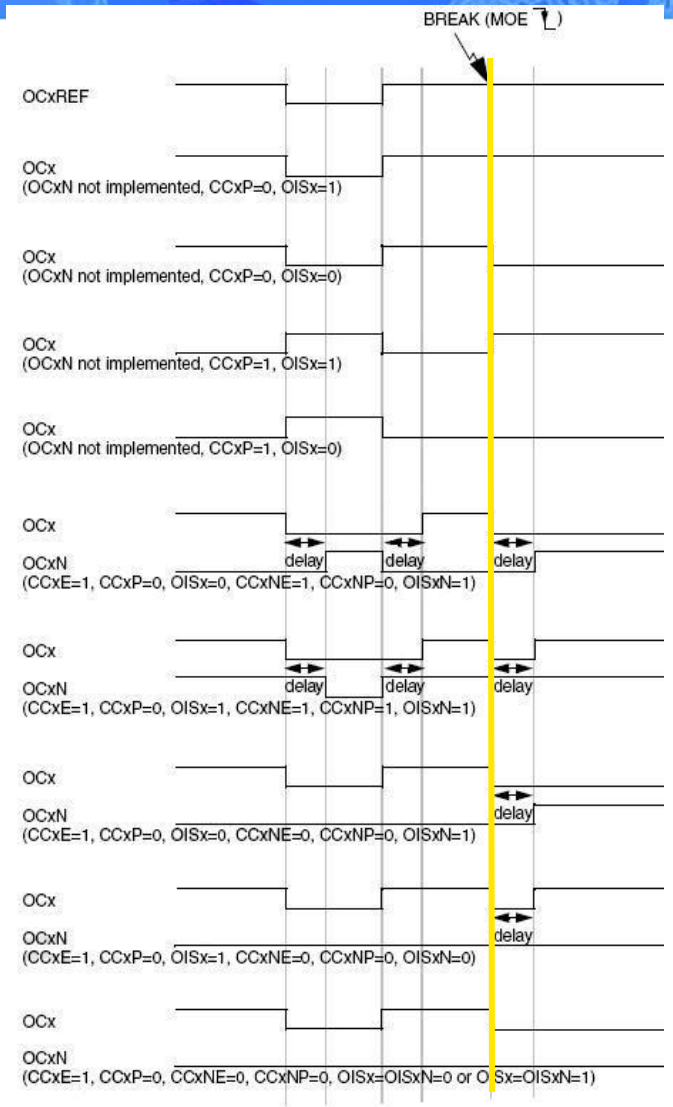
Complementary outputs & Dead time Insertion

- **This mode allows**
  - Outputs two complementary signals for each three channels.
  - Polarity can be selected independently
  - Manage the dead-time between the switching-off and the switching-on instants of the outputs.
- Reference waveform OCx_{REF} generates 2 outputs OCx and OCxN for the three channels.
  - OCx rising edge is delayed to **reference rising** edge
  - OCNx rising edge is delayed to **reference falling** edge





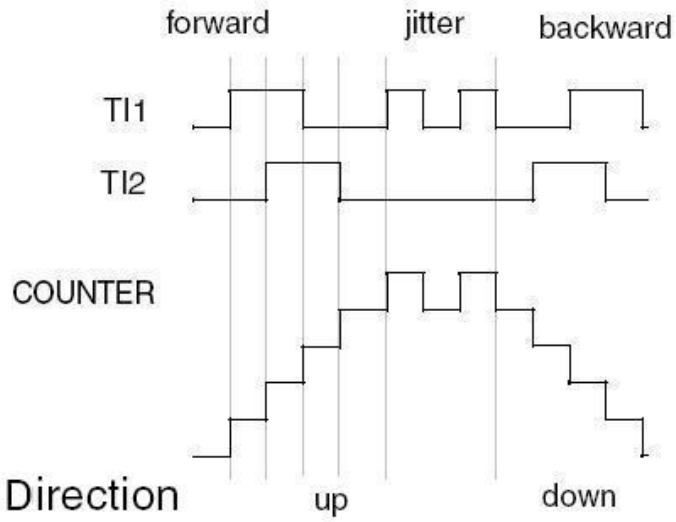
Output Control with Break



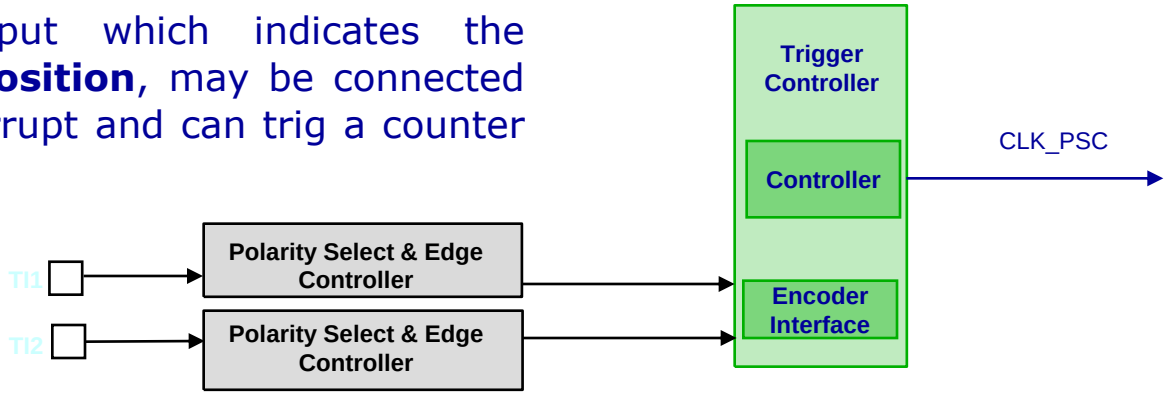
Control bits					Output states	
MOE bit	OSSI bit	OSSR bit	CCxE bit	CCxNE bit	OCx output state	OCxN output state
1	X	0	0	0	Output Disabled (not driven by the timer)	Output Disabled (not driven by the timer)
		0	0	1	Output Disabled (not driven by the timer)	OCxREF + Polarity OCxN=OCxREF xor CCxNP
		0	1	0	OCxREF + Polarity OCx=OCxREF xor CCxP	Output Disabled (not driven by the timer)
		0	1	1	OCREF + Polarity + dead-time	Complementary to OCREF (not OCREF) + Polarity + dead-time
		1	0	0	Output Disabled (not driven by the timer)	Output Disabled (not driven by the timer)
		1	0	1	Off-State (output enabled with inactive state) OCx=CCxP	OCxREF + Polarity OCxN=OCxREF xor CCxNP
		1	1	0	OCxREF + Polarity OCx=OCxREF xor CCxP	Off-State (output enabled with inactive state) OCxN=CCxNP
		1	1	1	OCREF + Polarity + dead-time	Complementary to OCREF (not OCREF) + Polarity + dead-time
0	0	X	0	0	Output Disabled (not driven by the timer)	
	0		0	1		
	0		1	0		
	0		1	1		
	1		0	0		
	1		0	1	Off-State (output enabled with inactive state) Asynchronously: OCx=CCxP, OCxN=CCxNP Then if the clock is present: OCx=OISx and OCxN=OISxN after a dead-time, assuming that OISx and OISxN don't correspond to OCX and OCxN both to active state	
	1		1	0		
	1		1	1		

Encoder Interface

- The **two inputs** TI1 and TI2 are used to interface to an incremental encoder **without** external interface **logic**.
- The sequence of transitions of the two inputs is evaluated and generates **count pulses** as well as the **direction** signal by hardware accordingly.
- The counter provides information on the current **position** and DIR control bit provides information on the encoder **direction.**

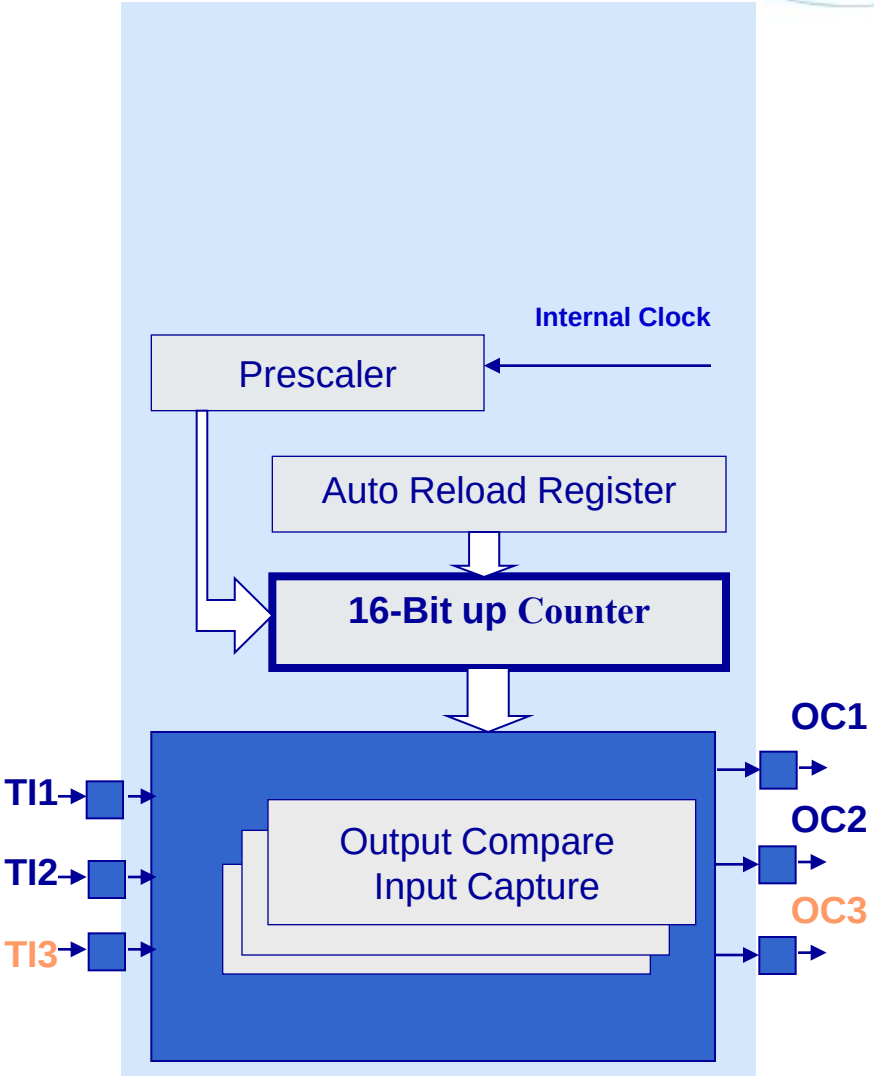


- The encoder output which indicates the mechanical **zero position**, may be connected to an external interrupt and can trig a counter reset.



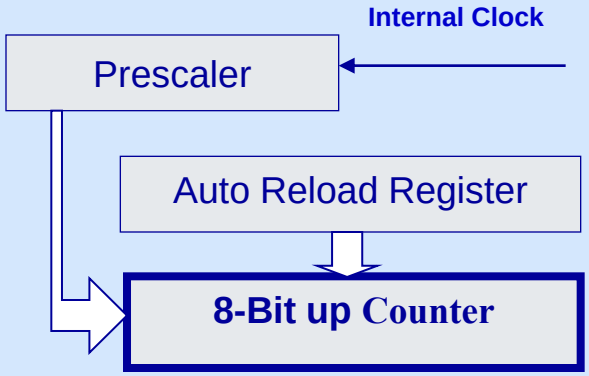
STM8S Timer 2,3 Features

- **16-bit Counter**
  - Up counting modes
  - Auto Reload
  - Programmable prescaler
- **2-3 x 16 bit Channel**
  - Input Capture
  - Output Compare
  - PWM (edge -aligned)
  - One pulse mode output
  - Forced output mode
- **Interrupts & Update Event**
  - Counter initialization
  - Input capture, Output compare



STM8S Timer 4 Features

- **8-bit Counter**
  - Up counting mode
  - Auto Reload
  - Programmable prescaler
- **Update Event & Interrupts**
  - Counter initialization



Quiz

- Up to how many TIM timers are available in the STM8 device?
- How many pins on the product are implemented per channel?
- What are the main counter clock sources?
- What can I measure with PWM input mode?

References

- RM0016 STM8S Reference Manual
- AN2658 Using ADC of STM8
- AN2719 Precision improvement of the STM8 ADC
- UM0709 STM8/128-MCKIT motor control starter kit

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